OIPE IAP38 SEP 06 2005 PATENT & TRADEMARK OFFICE

Patent
Attorney Docket No. 015290-755

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

COPY

In re Patent Application of
Michael Setton
Application No.: 10/622,484
Filing Date: July 21, 2003
Group Art Unit: 2812
Examiner: Ron Everett Pompey
Confirmation No.: 4980
Title: ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR

AMENDMENT/REPLY TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed is a reply for the above-identified patent application.

8-9-05 JS
A3

☐ A Petition for Extension of Time is also enclosed.

☐ Terminal Disclaimer(s) and the ☐ $65.00 (2814) ☐ $130.00 (1814) fee per Disclaimer due under 37 C.F.R. § 1.20(d) are also enclosed.

☐ Also enclosed is/are _____

☐ Small entity status is hereby claimed.

☐ Applicant(s) requests continued examination under 37 C.F.R. § 1.114 and enclose the ☐ $395.00 (2801) ☐ $790.00 (1801) fee due under 37 C.F.R. § 1.17(e).

☐ Applicant(s) requests that any previously unentered after final amendments not be entered. Continued examination is requested based on the enclosed documents identified above.

☐ Applicant(s) previously submitted _____
on _____,
for which continued examination is requested.

☐ Applicant(s) requests suspension of action by the Office until at least _____, which does not exceed three months from the filing of this RCE, in accordance with 37 C.F.R. § 1.103(c). The required fee under 37 C.F.R. § 1.17(i) is enclosed.

☐ A Request for Entry and Consideration of Submission under 37 C.F.R. § 1.129(a) (1809/2809) is also enclosed.

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☒ No additional claim fee is required.

☐ An additional claim fee is required, and is calculated as shown below.

AMENDED CLAIMS					
	No. of Claims	**Highest No. of Claims Previously Paid For**	**Extra Claims**	**Rate**	**Additional Fee**
Total Claims	14	MINUS 20 =	0	x $50.00 (1202) =	$ 0.00
Independent Claims	5	MINUS 5 =	0	x $200.00 (1201) =	$ 0.00
If Amendment adds multiple dependent claims, add $360.00 (1203)					
Total Claim Amendment Fee					$ 0.00
☐ Small Entity Status claimed - subtract 50% of Total Claim Amendment Fee					$ 0.00
TOTAL ADDITIONAL CLAIM FEE DUE FOR THIS AMENDMENT					**$ 0.00**

☐ A check in the amount of _____ is enclosed for the fee due.

☐ Charge _____ to Deposit Account No. 02-4800.

☐ Charge _____ to credit card. Form PTO-2038 is attached.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(d) and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By _____
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Date: August 9, 2005

Patent
Attorney's Docket No. 015290-755

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Michael SETTON	)	Group Art Unit: 2812
	)	
Application No.: 10/622,484	)	Examiner: Ron Everett Pompey
	)	
Filed: July 21, 2003	)	Confirmation No.: 4980
	)	
For: ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR	)	

AMENDMENT UNDER 37 C.F.R. § 1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In complete response to the Office Action dated June 6, 2005, Applicant submits herewith the following Response.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this Response.

Remarks begin on page 8 of this Response.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-37. (Canceled)

38. (Currently Amended) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, and wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer; [[and]]

(d) forming source and drain regions in the substrate adjacent to the gate electrode; and

(e) forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer.

39. (Previously Presented) The method of Claim 38 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

40. (Previously Presented) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, and wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer; and

(d) forming source and drain regions in the substrate adjacent to the gate electrode.

41. (Previously Presented) The method of Claim 40 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

42. (Previously Presented) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer; and

(d) forming source and drain regions in the substrate adjacent to the gate electrode.

43. (Previously Presented) The method of Claim 42 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

44. (Currently Amended) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming a silicon nitride interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the silicon nitride interfacial layer, the high dielectric constant layer comprising a material that is selected from the group consisting of Ta_2O_5, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, and mixtures thereof wherein the silicon nitride interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer; [[and]]

(d) forming source and drain regions in the substrate adjacent to the gate electrode; and

(e) forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer.

45. (Currently Amended) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising a material selected from the group consisting of

$Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6,

a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, and

a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1,

wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer; [[and]]

(d) forming source and drain regions in the substrate adjacent to the gate electrode; and

(e) forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer.

46. (Previously Presented) The method of Claim 38 wherein the interfacial layer comprises silicon oxide.

47. (Previously Presented) The method of Claim 38 wherein the interfacial layer comprises silicon nitride or silicon oxynitride.

48. (Canceled)

49. (Previously Presented) The method of Claim 45 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

50. (New) The method of Claim 38 wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate.

51. (New) The method of Claim 44 wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate.

52. (New) The method of Claim 45 wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate.

REMARKS

Status of the Claims

Claims 38-47 and 49-52 are pending, with Claims 38, 40, 42, 44, and 45 being independent. Claims 50-52 have been added and Claims 38, 44, and 45 have been amended. Specifically, Claims 38, 44, and 45 have been amended to recite "forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer.". Support for the new claims and amendments may be found throughout the specification and claims as originally filed. No new matter has been added.

Initially, Applicant would like to thank the Examiner for indicating that Claims 40-43 are allowed.

Applicant notes that while the Office Action Summary indicates that Claim 49 is rejected, Claim 49 does not appear in pages 2-5 of the Office Action. Applicant assumes that the rejection under 35 U.S.C. § 103 of Claims 38, 39, and 44-48 is meant to read Claims 38, 39, 44-47, and 49.

Applicant respectfully requests the Examiner to reconsider and withdraw the outstanding rejections in view of the foregoing amendments and following remarks.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 38, 39, and 44-48 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,880,508 ("Wu") in view of admitted prior art

("APA") or U.S. Patent No. 4,947,081 ("Ohiwa"). This rejection is respectfully traversed.

Wu is cited as allegedly disclosing the steps of:

> "forming an interfacial layer (6, fig. 1), comprising silicon nitride or silicon oxynitride, on a silicon semiconductor substrate; and
> forming a high dielectric constant layer (8, fig. 1) on the interfacial layer;
> forming a gate electrode of an electrically conductive material on the high dielectric constant layer; and
> forming source and drain regions that are adjacent the gate electrode. (col. 2, lns. 63-67 and col. 3, lns. 1-22)." (Official Action at page 2).

Initially, the Examiner is requested to cite specific portions of any prior art references encompassed by the alleged APA and explain where any such prior art provides the requisite motivation or incentive to modify Wu in a manner which would result in the various combinations of features recited in independent Claims 38, 44, and 45. Further, it is not seen where the alleged disclosure of a silicon nitride interfacial layer is found in Wu. As such, the Examiner is requested to identify the portion of Wu considered to disclose a silicon nitride interfacial layer.

Wu relates to a method of fabricating a metal oxide semiconductor field effect transistor (MOSFET) with a permitivity gate dielectric. (Column 1, Lines 7-10). Wu discloses forming an ultra thin silicon oxynitride layer 6 on the top surface of a single crystal silicon substrate. (Column 2, Lines 51-67). Wu further discloses depositing a thin dielectric layer 8 with high permitivity by chemical vapor deposition on the silicon oxynitride layer. (Column 3, Lines 1-4). As disclosed by Wu, the dielectric layer can be

chosen from a group of TiO_2, Ta_2O_5, PZT or BST, which have relatively high dielectric to silicon oxide, silicon nitride or the like. (Column 3, Lines 4-7). The layers 6, 8 form a gate dielectric. (Column 3, Lines 30-31). Wu uses the gate structure as a mask to form shallow source and drain junctions adjacent the gate and sidewall spacers 18 are formed on the side walls of the gate structure and upper surface of the silicon substrate. (Column 3, Lines 33-36).

Referring to FIG. 4, the side wall spacers of Wu are only on the side walls of the gate structure. (Column 3, Lines 34-36). Wu removes portions of the gate dielectric such that the spacers are formed on an upper surface of the silicon substrate 2. Thus, Wu teaches away from forming the spacers on the upper surface of the dielectric layer 8.

The Office Action acknowledges that Wu fails to disclose a high dielectric layer comprising $Ta_2(O_{1-x}N_x)_5$ and a gate width of less than 0.3 microns. Accordingly, the alleged APA on page 6, lines 24-26 of the present specification and Ohiwa are cited as allegedly disclosing that a high dielectric layer can be formed of $Ta_2(O_{1-x}N_x)_5$. (Office Action at page 2). With regard to the APA, the rejection does not identify the portions of any prior art reference relied on to reject independent Claims 38, 44, and 45.

Ohiwa relates to a thin film electroluminescence device having dual insulation layers. (Column 1, Lines 8-9). Ohiwa discloses that a tantalum oxynitride layer 3 is deposited on an indium tin oxide (ITO) electrode layer 2 and that an insulating layer 4, which can be Ta_2O_5, is deposited on layer 3. In contrast, Wu deposits dielectric layer 8 of Ta_2O_5, TiO_2, PZT, or BST on silicon oxynitride layer 6. Thus, Ohiwa does not provide a

tantalum oxynitride layer on an interfacial layer nor does Ohiwa teach equivalency of Ta_2O_5 and tantalum oxynitride since Ohiwa adds a tantalum oxynitride layer to a Ta_2O_5 layer. Moreover, Ohiwa relates to a completely different field than Wu and clearly is not pertinent to any problem sought to be solved by Wu.

I. Ohiwa Is Non-Analogous Prior Art

"In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). MPEP § 2141.01(a).

Applicant respectfully submits that Ohiwa, related to a thin film electroluminescence device classified in class 313, is nonanalogous art to the transistor of Wu classified in class 257. As such, Ohiwa may not be relied upon as a basis for rejection of the presently claimed methods. Applicant further respectfully submits that Ohiwa is not reasonably pertinent to the particular problem with which the inventor was concerned, methods for fabricating integrated circuits using metal oxide semiconductor (MOS) technology. (Page 1, Lines 4-5). Accordingly, because Ohiwa is non-analogous prior art, the rejection should be withdrawn.

II. **No *Prima Facie* Case of Obviousness Has Been Established**

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 2143.

Applicant respectfully submits that there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine Wu, related to a method of fabricating a MOSFET with a permitivity gate dielectric, and Ohiwa, related to a thin film electroluminescence device. Applicant further respectfully submits that there is no reasonable expectation of success in combining Wu and Ohiwa. In particular, as noted above, Wu discloses depositing a dielectric layer on a silicon oxynitride layer formed on a silicon substrate, whereas Ohiwa discloses providing a tantalum oxynitride layer between a first insulation layer and a transparent electrode. Ohiwa provides a layer of tantalum oxynitride on an indium tin oxide (ITO) layer for purposes of preventing diffusion of oxygen into the ITO layer during formation of a Ta_2O_5 layer. (Column 2, Lines 3-22). As Ohiwa has nothing to do with MOSFET devices, there is no motivation to combine the two references absent impermissible hindsight. However, even if Wu and Ohiwa are combined, the resulting combination fails to suggest the

combination of steps recited in independent Claims 38, 44, and 45, which includes forming spacers on an upper surface of the high dielectric constant layer.

A. **Claims 38, 39, 45-47, 49, 50, and 52**

Independent Claim 38 recites a method for fabricating a MOS device having a gate width of less than 0.3 micron comprising forming an interfacial layer on a semiconductor substrate. A high dielectric constant layer is formed on the interfacial layer, the high dielectric constant layer comprising $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, and wherein the interfacial layer separates the high dielectric constant layer from the substrate. A gate electrode of an electrically conductive material is formed on the high dielectric constant layer. Spacers are formed adjacent to the gate electrode and on an upper surface of the high dielectric constant layer. Claims 39, 46, 47, and 50 are dependent upon independent Claim 38.

Independent Claim 45 recites a method for fabricating a MOS device having a gate width of less than 0.3 micron comprising forming an interfacial layer on a semiconductor substrate. A high dielectric constant layer is formed on the interfacial layer, the high dielectric constant layer comprising a material selected from the group consisting of $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, and a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, wherein the interfacial layer separates the high dielectric constant layer from the substrate. A gate electrode of an

electrically conductive material is formed on the high dielectric constant layer. Spacers are formed adjacent to the gate electrode and on an upper surface of the high dielectric constant layer. Claims 49 and 52 are dependent upon independent Claim 45.

As noted above, Applicant respectfully submits that: (1) Ohiwa is nonanalogous art to the transistor of Wu; (2) Ohiwa is not reasonably pertinent to the particular problem with which the inventor was concerned; (3) there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine Wu and Ohiwa; and (4) there is no reasonable expectation of success in combining Wu and Ohiwa.

Applicant additionally respectfully submits that the combination of Wu and Ohiwa does not teach or suggest all the claim limitations of Claims 38, 39, 45-47, and 49, as it is unknown how the tantalum oxynitride layer provided between a first insulation layer and a transparent electrode of Ohiwa is to be combined with the dielectric layer of Wu to provide the presently claimed high dielectric constant layer comprising $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6. In particular, with regard to combining Wu and Ohiwa, the Office Action simply asserts that "it would have been obvious to one of ordinary skill in the art to combine ... Ohiwa with Wu, because the above listed materials are art equivalent high dielectric material with Ta_2O_5 of the Wu reference." (Page 3). On the contrary, although Ohiwa is non-analogous art, Ohiwa adds tantalum oxynitride to a Ta_2O_5 containing electroluminescent device to achieve an effect not provided by Ta_2O_5 alone. Thus, Ohiwa shows non-equivalency of Ta_2O_5 and tantalum oxynitride.

Applicant further respectfully submits that the combination of Wu and Ohiwa does not teach or suggest all the claim limitations of Claims 38, 39, 45-47, and 49, for, as noted above, Wu does not teach or suggest forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer, as recited in independent Claims 38 and 45. Ohiwa, cited as allegedly disclosing that a high dielectric layer can be formed of $Ta_2(O_{1-x}N_x)_5$, does not cure the deficiencies of Wu in this regard.

In addition, Applicant respectfully submits that the combination of Wu and Ohiwa does not teach or suggest all the claim limitations of Claims 50 and 52, for, as noted above, Wu removes portions of the gate dielectric such that the spacers are formed on an upper surface of the silicon substrate. In contrast, Claims 50 and 52 recite that the interfacial layer and the high dielectric constant layer separates the spacers from the substrate. Ohiwa, cited as allegedly disclosing that a high dielectric layer can be formed of $Ta_2(O_{1-x}N_x)_5$, does not cure the deficiencies of Wu in this regard.

Accordingly, for at least the above-noted reasons, Applicant respectfully submits that the Office Action has not set forth a *prima facie* case of obviousness. Accordingly, withdrawal of the rejection is respectfully requested.

B. **Claims 44 and 51**

Independent Claim 44 recites a method for fabricating a MOS device having a gate width of less than 0.3 micron comprising forming a silicon nitride interfacial layer on a semiconductor substrate. A high dielectric constant layer is formed on the silicon nitride

interfacial layer, the high dielectric constant layer comprising a material that is selected from the group consisting of Ta_2O_5, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, and mixtures thereof wherein the silicon nitride interfacial layer separates the high dielectric constant layer from the substrate. A gate electrode of an electrically conductive material is formed on the high dielectric constant layer. Source and drain regions are formed in the substrate adjacent to the gate electrode. Spacers are formed adjacent to the gate electrode and on an upper surface of the high dielectric constant layer. Claim 51 is dependent upon independent Claim 44.

Wu fails to disclose a MOSFET having a silicon nitride interfacial layer. While the Office Action asserts that Wu discloses "forming an interfacial layer (6, fig. 1), comprising silicon nitride or silicon oxynitride, on a silicon semiconductor substrate," Applicant points out that Wu only discloses forming a silicon oxynitride interfacial layer. Specifically, Wu discloses forming a silicon oxynitride layer on the top surface of a single crystal silicon substrate and depositing a thin dielectric layer with high permitivity on the silicon oxynitride layer.

Thus, Applicant further respectfully submits that the combination of Wu and Ohiwa does not disclose or suggest all the claim limitations of Claim 44. In particular, Wu does not disclose or suggest forming a silicon nitride interfacial layer on a semiconductor substrate and, as noted above, Wu does not teach or suggest forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer. Ohiwa, cited

as allegedly disclosing that a high dielectric layer can be formed of $Ta_2(O_{1-x}N_x)_5$, does not cure the deficiencies of Wu in this regard.

In addition, Applicant respectfully submits that the combination of Wu and Ohiwa does not teach or suggest all the claim limitations of Claim 51, for, as noted above, Wu removes portions of the gate dielectric such that the spacers are formed on an upper surface of the silicon substrate. In contrast, Claim 51 recites that the interfacial layer and the high dielectric constant layer separates the spacers from the substrate. Ohiwa, cited as allegedly disclosing that a high dielectric layer can be formed of $Ta_2(O_{1-x}N_x)_5$, does not cure the deficiencies of Wu in this regard.

Accordingly, for at least the above-noted reasons, Applicant respectfully submits that the Office Action has not set forth a *prima facie* case of obviousness. Accordingly, withdrawal of the rejection is respectfully requested.

Conclusion

For the reasons noted above, the art of record does not disclose or suggest the inventive concept of the presently claimed invention as defined by the claims.

In view of the foregoing amendments and remarks, reconsideration of the claims and allowance of the subject application is earnestly solicited. The Examiner is invited to contact the undersigned at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: August 9, 2005

By: _____
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